HDMI to FMC Module

User Guide

Rev. 1.0**.**38 **-** 26 February 2019

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References

[1] ANSI_VITA_57DOT1 - FMC Standard : The PCB dimensions and FMC connector pinout can be found in this document.

[2] Intelligent Platform Management interface specification, second generation. The document can be downloaded from http://www.intel.com/design/servers/ipmi/

Revision History

Revision	Modifications
1.0.10	• Original revision
1.0.38	• Update of legal and brand name

HMDI to FMC Module

Introduction

The EA-HDMI-FMC-01 module is an EXOSTIV™ adapter board converting HDMI type-A receptacle connector to FMC terminal (male) array assembly connector.

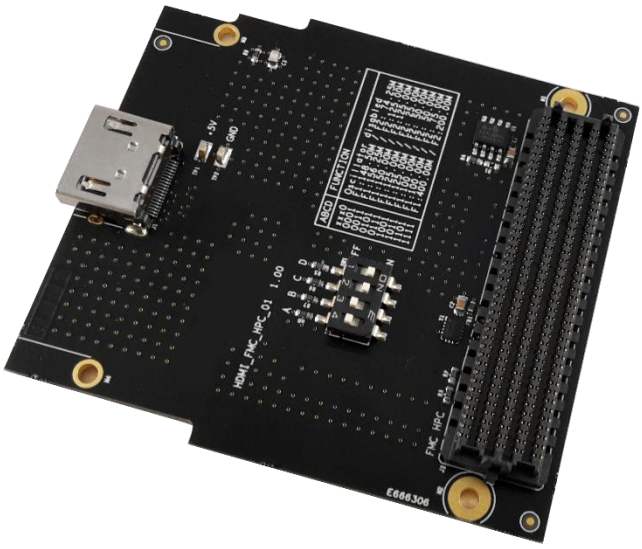


Figure 1: EA-HDMI-FMC_01 adapter from Exostiv Labs

This module is compatible with the ANSI VITA specification 57.1 (refer to [1]). The module physical dimensions, the connector position and pin assignments are implemented as defined in this standard.

Using the EA-HDMI-FMC-01 module gives the possibility to connect the EXOSTIV™ probe to any board using FMC-LPC and/or FMC-HPC connector. One or two of these interfaces can be found on all development board of Xilinx 7 series FPGA.

Note: 1. In this document, the MODULE board refers to the EA-HDMI-FMC module board and the CARRIER board refers to the target board of the system under tests on which the module is plugged (as defined by the FMC standard).

Features

- Standard single width FMC module dimensions
- Up to 4 transceiver upstream links when using FMC-HPC interface
- Single transceiver upstream link when using FMC-LPC interface
- On-board dual transceiver reference clock with selectable frequencies
- I²C bus for downstream link
- On-board I²C pull-up resistor
- FMC plug connector to interface the system under test.
- HDMI type A receptacle to interface EXOSTIV™ Probe
- IPMI EEPROM for ANSI VITA standard compliance

Physical Dimensions

The PCB physical dimensions are compliant with the ANSI VITA standard 57.1 (refer to [1]). The overall module dimensions are 76.5 mm x 69.0 mm x 8.7 mm (L x W x H).

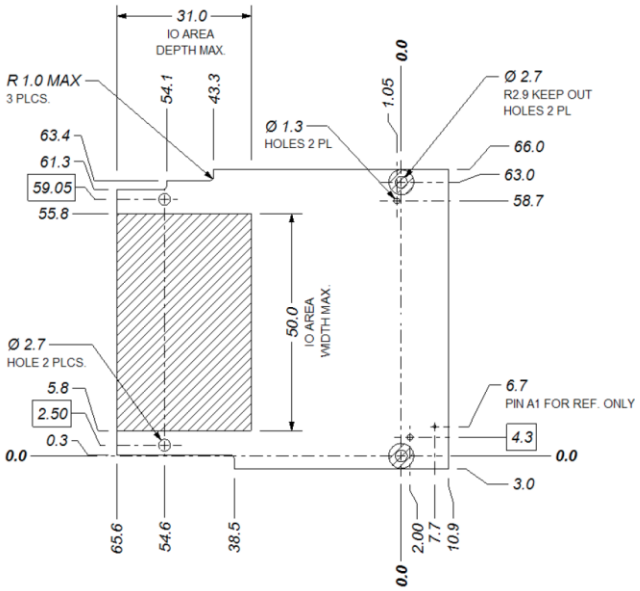
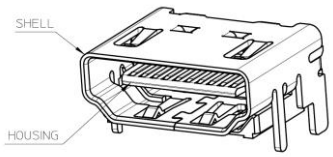


Figure 2: PCB dimensions (all dimensions in mm)

HDMI Connector

The HDMI connector of the EA-HDMI-FMC-01 module is used to connect the EXOSTIV™ probe EP3000-X, EP6000-X and EP12000-X series.



Data are transferred through the HDMI connector. Up to 4 transceiver links for upstream link can be used to collect the samples captured from inside the system under test. A low speed I²C bus is used for the downstream link to configure the EXOSTIV™ IP inserted in the target FPGA (refer to the "**Error! Reference source not found.**" section for more details). The HDMI power line is not used on this module.

Notes: 1. Even if an industry standard HDMI connector is used on the EA-HDMI-SFP-01 adapter, do not connect any HDMI-compatible device to it. The multi-gigabit transceiver port of the EA-HDMI-SFP-01 adapter is not pin and functionality-compatible with the HDMI video standard.

FMC Connector

The FMC connector is a 400 pins high density array male connector. Table provides the SAMTEC part number for the on-board male connector and the corresponding female mating parts. The EA-HDMI-FMC-01 module is equipped with a high pin count connector. The mating stack height is equal to 10 mm.
The connector pins are organised in a matrix of 10 columns of 40 pins each. Column are identified as A, B, C, D, E, F, G, H, J, K and pins are indexed from 1 to 40. Two types of FMC connectors are available. The high pin count version (HPC) is fully populated and has 400 pins. The low pin count version (LPC) only has 160 pins populated in columns C, D, G and H.

Figure 3: FMC mating connectors

Table 1: SAMTEC[1] FMC part numbers

SAMTEC Part Number	VITA Part Number	Description	Mated Stack Height	Pin Count
ASP-134486-01	CC-HPC-10	Female		High
ASP-134603-01	CC-LPC-10	Female		Low
ASP-134602-01	MC-HPC-8.5	Male	8.5 mm	High
ASP-134606-01	MC-LPC-8.5	Male	8.5 mm	Low
ASP-134488-01[2]	MC-HPC-10	Male	10 mm	High
ASP-134604-01	MC-LPC-10	Male	10 mm	Low

1. MOLEX also has compatible parts.
2. Part mounted on module EA-HDMI-FMC-01

The *EA-HDMI-FMC-01* module is equipped with a high pin count FMC connector (FMC-HPC). When plugged into a mating high pin count female connector, the 4 transceiver links are available to transfer samples to the EXOSTIV™ probe. When plugged into a mating low pin count female connector, a single transceiver link can be used. The following tables describe the signals available through he FMC connector, their pin position, the reference voltages and their recommended DC levels.

Table 2: FPC connector signal list

Signal	HPC Pin	LPC Pin	Description
GBTCLK0_M2C_P	D4	D4	Primary LVDS differential clock used as reference clock for gigabit transceivers.
GBTCLK0_M2C_N	D5	D5	
GBTCLK1_M2C_P	B20	-	Secondary LVDS differential clock used as reference clock for gigabit transceivers.
GBTCLK1_M2C_N	B21	-	
DP0_C2M_P	C2	C2	Upstream transceiver link 0
DP0_C2M_N	C3	C3	
DP1_C2M_P	A22	-	Upstream transceiver link 1
DP1_C2M_N	A23	-	
DP2_C2M_P	A26	-	Upstream transceiver link 2
DP2_C2M_N	A27	-	
DP3_C2M_P	A30	-	Upstream transceiver link 3
DP3_C2M_N	A31	-	
LA00_P_CC	G6	G6	Downstream SCL line. Referenced to VADJ
LA00_N_CC	G7	G7	Downstream SDA line. Referenced to VADJ
PRSNT_M2C_L	H2	H2	Module presence detection. Connected to GND on module
SCL	C30	C30	SCL line reserved for IPMI EEPROM. Referenced to 3P3VAUX
SDA	C31	C31	SDA line reserved for IPMI EEPROM. Referenced to 3P3VAUX
GA0	C34	C34	Geographic module address bit 0.
GA1	D35	D35	Geographic module address bit 1.
TDI	D30	D30	JTAG data lines. As there is no JTAG chain on the module, these two pins are shorted together on the module as recommended by the VITA 57 standard [1].
TDO	D31	D31	
VADJ	E39,F40, G39,H40	G39,H40	Voltage level provided by the carrier board used for the on-board LVDS dual output oscillator
3P3VAUX	D32	D32	Voltage level provided by the carrier board used for the IPMI EEPROM.

Notes:
1. *Signal suffix _C2M indicates a signal driven by the carrier board and going to the module board.*
2. *Signal suffix _M2C indicates a signal driven by the module and going to the carrier board.*
3. *Complete HPC and LPC connector pinout can be found in the VITA 57 standard [1].*
4. *All signals not listed in Table are not connected (floating).*
5. *All GND connections recommended in the VITA 57 standard [1] are implemented on the module.*

Table 3: Recommended DC characteristics for VADJ

Parameters	Min	Typ	Max	Units	Notes
Supply voltage level	+1.71		+3.465	V	1.8V to 3.3V ± 5%
Supply current (I_{dd})		41	50	mA	

Table 4: Recommended DC characteristics for 3P3VAUX

Parameters	Min	Typ	Max	Units	Notes
Supply voltage level	+3.135	3.3	+3.465	V	3.3V ± 5%
Supply current (I_{dd})		3	5	mA	

I²C Bus

When using the HDMI connector, the downstream communication (from the EXOSTIV™ probe to the target system) is implemented with the dedicated I²C serial bus of the HDMI connector. This link is used to control the IP that is embedded in the FPGA fabric. The EXOSTIV™ probe operates as the bus master and the target system as the slave. SCL and SDA lines must be connected to user IO pins of the FPGA (refer to section "**Error! Reference source not found.**" to determine the position of these signals on the FMC connector).

The electrical levels of the I²C bus are referenced from the FMC connector ground level to the VADJ voltage level provided by the carrier board (target board under test) through the FMC connector pins. The pull-up resistors required for the correct operation of the SCL and SDA lines are mounted on the EA-HDMI-FMC-01 module.

Table 5: I²C bus specifications through HDMI connector

Parameter		Min	Typ	Max	Unit
Voltage reference	V_{ADJ}	1.8V	-	3.3V	V
SCL/SDA pull-up resistor (1%)	-	-	2.2	-	kΩ
SCL/SDA voltage level (within EXOSTIV™ probe)					
Low-level	V_{IL}	-0.5	-	0.85	V
High-level	V_{IH}	2.31	-	6	V
Low-level output current	I_{OL}	3	9	-	mA

Frequency Selectable Oscillator

As defined in the ANSI VITA standard [1] the module must provide the reference clock for the transceiver links. A low jitter dual output oscillator is mounted on the EA-HDMI-FMC-01 module. The frequency of the oscillator is digitally selectable and can be changed by the user using the on-board DIP switch. The two generated clock signals are LVDS differential pairs and must be terminated to 100Ω resistor on the destination board. This termination resistor is generally available as internal differential termination inside the FPGA. The oscillator output is directly routed to the connector pin without any AC coupling capacitors.

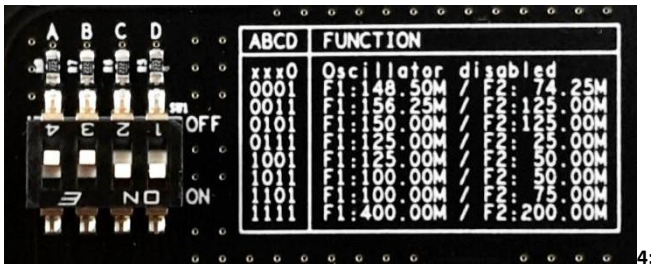


Figure 4: DIP switch to select oscillator frequencies

Refer to Figure for the definition of the DIP switch indexes. The 4 switches are referenced from A to D.
Switch D is used to turn the dual oscillator ON or OFF. When D is set in OFF position, both clock signals are set to high impedance state with a pull-up resistor of 40kΩ. When D is set to ON position, both clock signals are enabled. Their frequency is defined by switches A to C (refer to Table). A is the MSB (left bit) of the 3-b selection word. C is

the LSB (right bit). When a switch is set to ON position, a logic 1 is defined. When set to OFF position, a logic 0 is defined.

Table 6: Oscillator output frequencies

Frequency		000	001	010	011	100	101	110	111
GBTCLK0_M2C_P/N	MHz	148.50	156.25	150.00	125.00	125.00	100.00	100.00	400.00
GBTCLK1_M2C_P/N	MHz	74.25	125.00	125.00	25.00	50.00	50.00	75.00	200.00

Refer to section "**Error! Reference source not found.**" to determine the position of the transceiver reference clock signals. When the module is plugged on FMC-HPC connector, both clock are available. When plugged on FMC-LPC connector, only the first clock GBTCLK0_M2C_P/N is available.

Table 7: Oscillator specifications

Parameters	Min	Typ	Max	Units	Notes
Overall Frequency Stability	-50		50	ppm	
Supply voltage	+2.25		+3.6	V	
Startup time			5	ms	
Supply current (I_{dd})		38		mA	RL=100Ω, F1=F2=156.25MHz
Disable current		21	23	mA	Both outputs as tri-state (HiZ)
Output offset voltage	1.125		1.4	V	RL=100Ω differential
Peak—peak output swing		350		mV	Single-ended
Rise time		200	350	ps	RL=100Ω differential CL=2pF 20% to 80%
Fall time		200	350	ps	
Duty cycle	48		52	%	differential
Periodic jitter RMS		2.5		ps	F1=F2=156.25MHz
Integrated phase jitter		0.4	2	ps	100kHz~20MHz @ 156.25MHz

IPMI EEPROM

As described in the ANSI VITA standard [1], an EEPROM is mounted on board to support the Intelligent Platform Management Interface (IPMI EEPROM).
As most system do not need to support the IPMI specification, by default this EEPROM is blank. Contact Exostiv Labs at support@exostivlabs.com to load any particular content in this EEPROM. For more details on the EEPROM content refer to [2].

The EEPROM is power from the 3P3VAUX voltage level provided by the carrier board.

The EEPROM I²C slave address is function of the geographic address bits provided by the carrier. The level of GA1 and GA0 are defined on the carrier board by connecting these pins directly to 3P3VAUX or GND. The maximum I²C bus operating frequency is limited to 400 kHz.

Table 8: IPMI EEPROM slave address

GA[1:0]	I²C Slave Address
00	0b101 0000
01	0b101 0001
10	0b101 0010
11	0b101 0011

Notes: 1. The pull-up resistors required for the I²C clock and data lines must be foreseen on the carrier board and be connected to 3P3VAUX.

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